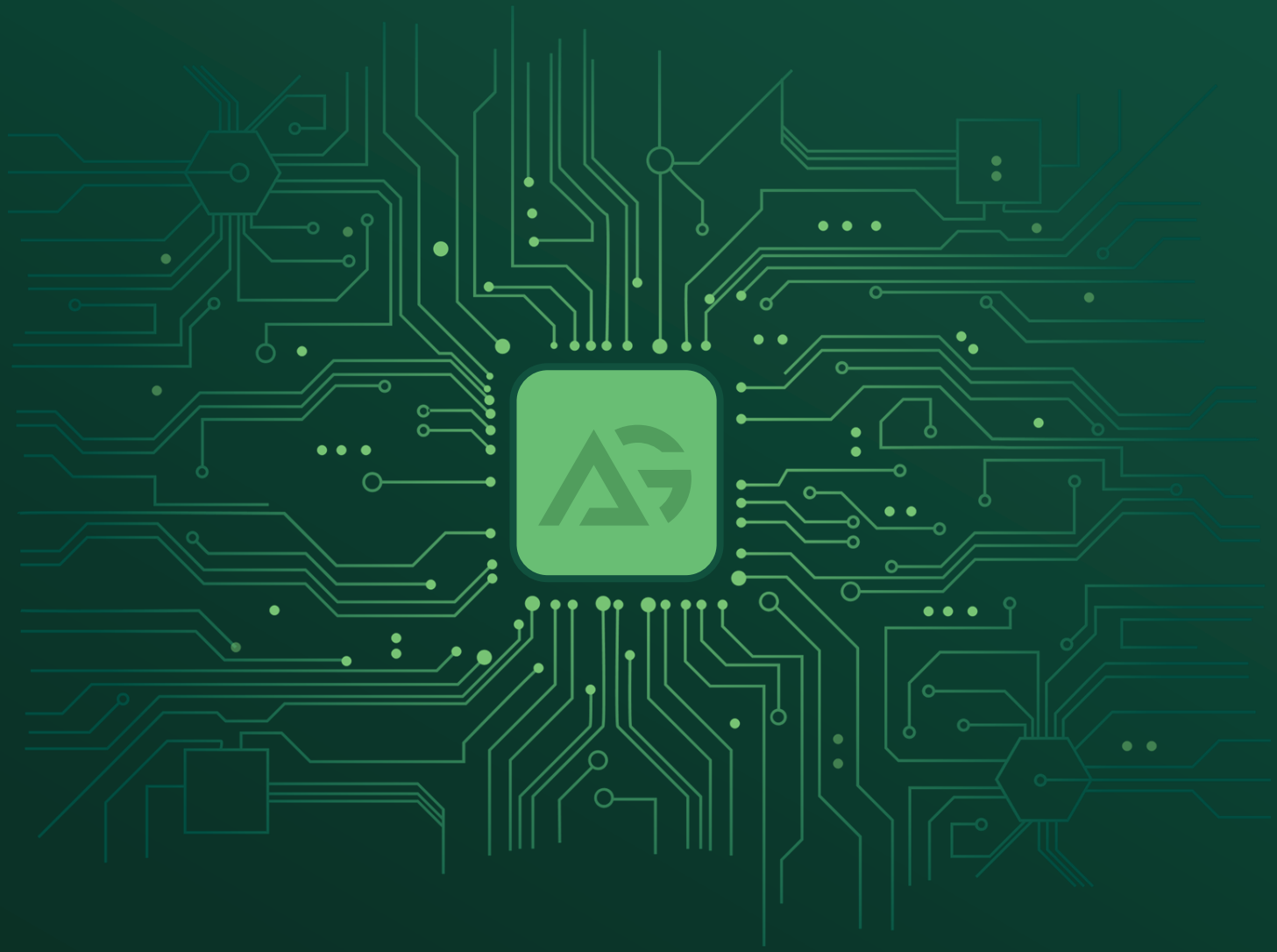
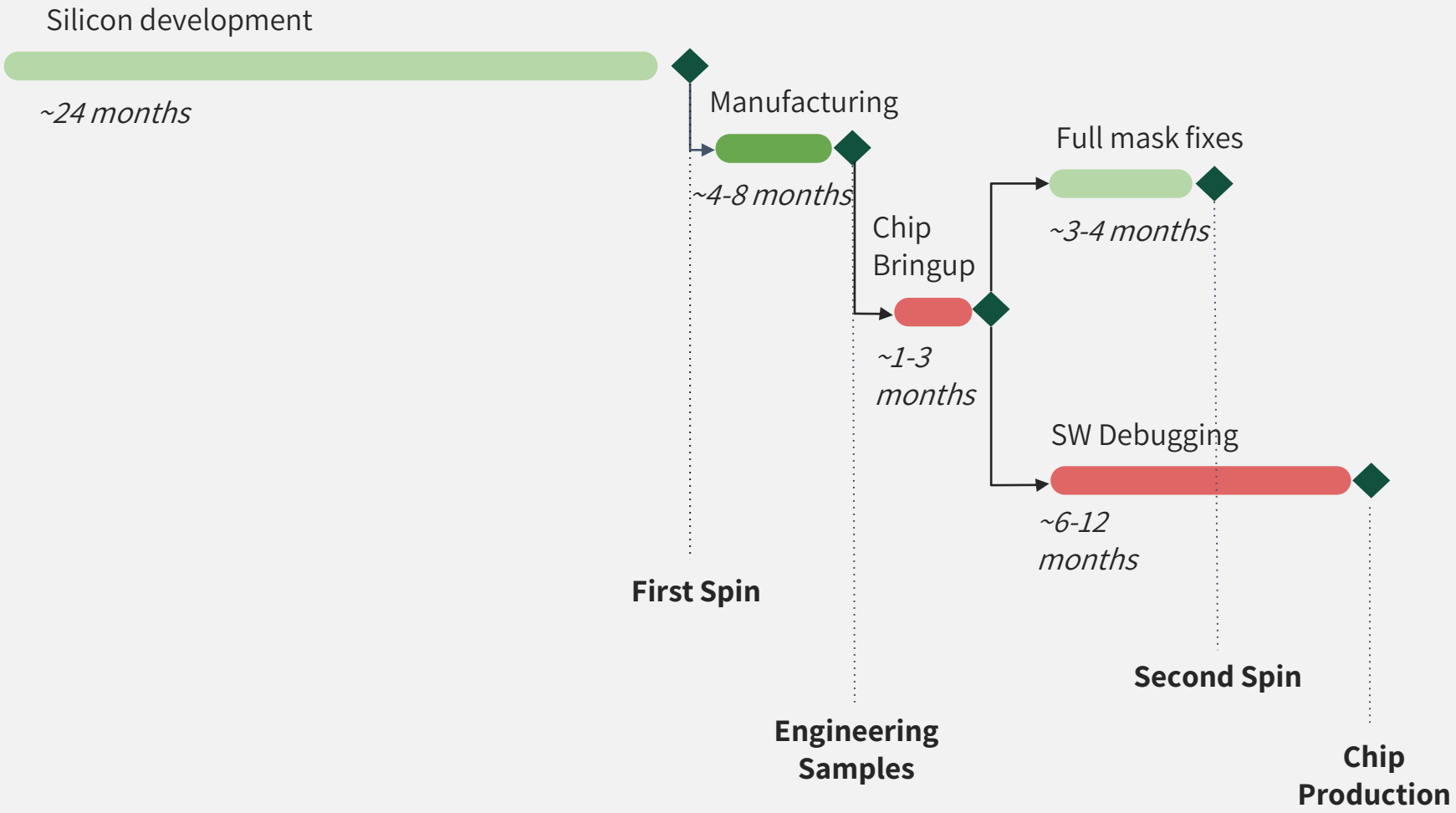
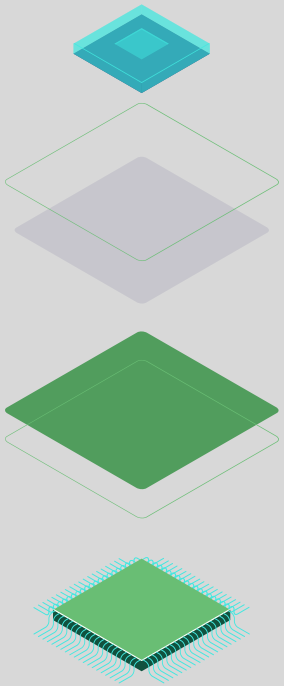


AsicGram

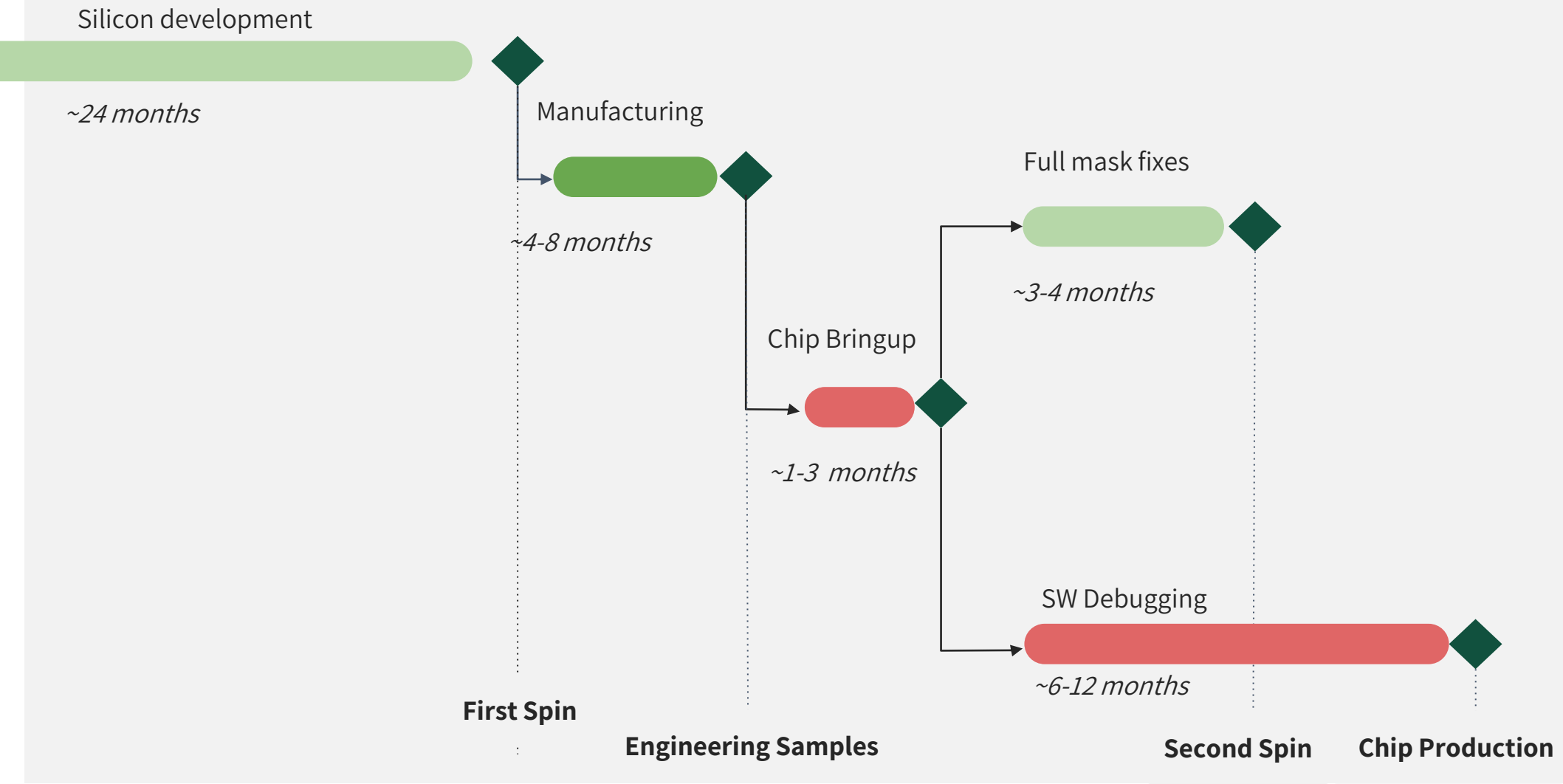
The Gold Standard for Silicon Debug

The Need


Silicon development
~24 months
Manufacturing
~4-8 months
Chip Bringup
~1-3 months
Full mask fixes
~3-4 months
SW Debugging
~6-12 months
First Spin
Engineering Samples
Second Spin
Chip Production



The Need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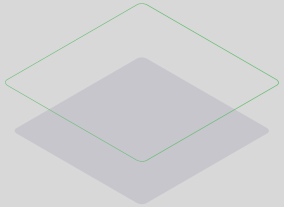
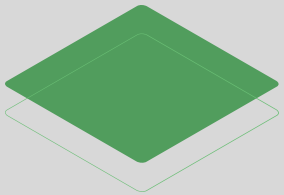
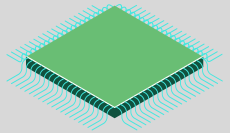
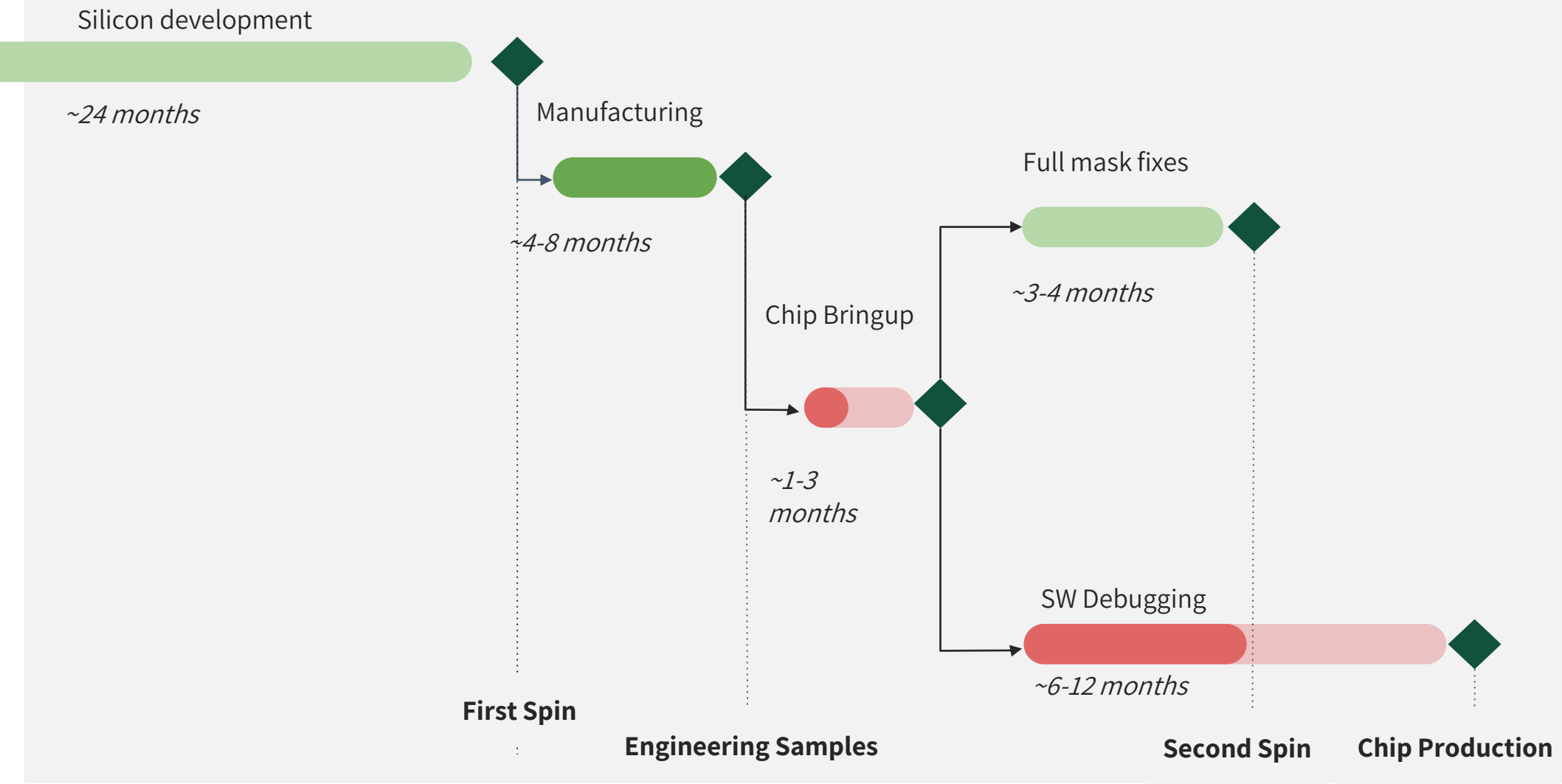






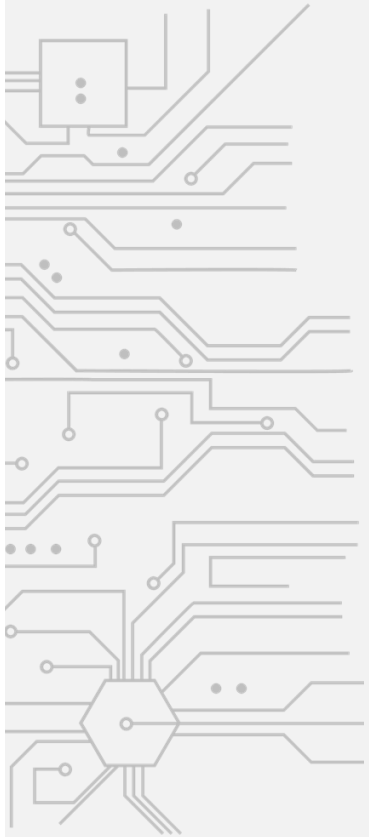
The Need



Lack of internal visibility results in long HW & SW debug iterations

Accelerating debug time shortens time-to-market

Value Proposition



Time-to-market

Reducing **1-3 months** (bringup and SW debug) which can be the difference between winning or missing the market

Engineering resources

Saving **20-30%** of post-silicon debug time and **2-5%** of overall project cost

Improved chip quality

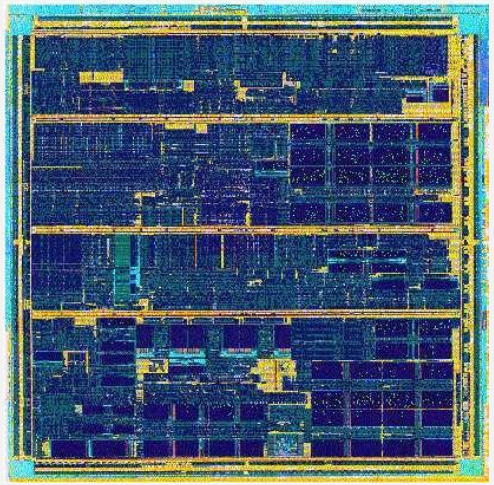
Avoiding re-spins which can cost **5-30M$** (for a full mask set) per spin and delay time-to-market by **4-8 months**

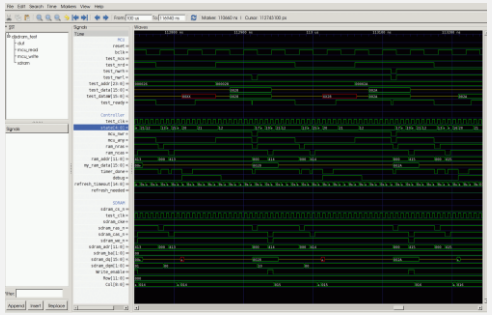
inVivo™: Obtaining Chip Sonogram

inVivo IP
is inserted into the chip during the development stage while minimizing overhead

inVivo SW
tools connect to the chip after fabrication and obtain visibility into events, signals and data

Scale
Fits any digital chip, scales from small-chips to multi-chiplet SoCs





Plug and Play
integration into the chip

Connect to the Chip
through Intuitive GUI

Silicon Validation Market

DFT
Design For Test

cadence
SIEMENS
SYNOPSYS

DFD
Design For Debug

SIEMENS

DFM
Design For Manufacturing

proteanTecs
SYNOPSYS

Wafer, component and PCB **Inspection**

APPLIED MATERIALS
KLA
NOVAMI
HEXAGON
Cybord
OMRON
ADVANTEST
TERADYNE

TAM

Potential value of **5B$**
(3.9B$ in licensing and
1.1B$ in royalties)

Competition

Dominated by home grown solutions challenged by **ease-of-use** and **ease-of-integration**

Product Comparison

Category	Sub Category	Home Grown	UltraSoC/Siemens	inVivo™
Features	Logic Analyzer	✓	✓	✓
	Smart Capture (events, transactions)	✗	✗	✓
	Data Compression	✗	✓	✓
	Performance Monitoring	✗	✓	✓
	Health Provisioning	✗	✗	✓
	Automated Testing	✗	✗	✓
	Advanced Triggers	✗	✗	✓
	HW/SW co-debug	✗	✓	✓
	Tap-point Recommendation Engine	✗	✗	✓
	Ease of RTL Integration (auto instrumentation)	✗	✗	✓
	Advanced GUI	✗	✗	✓
Cost		**300-600K$/year**	**300K$/chip**	**300K$/chip**

Better product than Home Grown solutions

Cheaper solution than internal development

Business Strategy

Pricing

License **$300K**/chip
(2 spins)

Software license/user
$30K per year

Royalties
(0.1-0.5% unit cost)

Focus

Start with small and medium companies (faster decision making, less demanding)

Drive proliferation

Identifying strategic partners for fine tuning of the product

Establish

inVivo ™
as industry **gold standard** and approach big names

Management Team

Run by seasoned global industry leaders, with tech, entrepreneurship and real estate backgrounds.

Arik Shmayovitsh
Founder & CEO

Gadi Laufer
Founder & CTO

Amir Hasidim
Chairman

Ran Laufer
CMO

Avraham Hampel
CFO

CEVA · cadence · GlobespanVirata · ENTROPIC · IBM · COPPERGATE

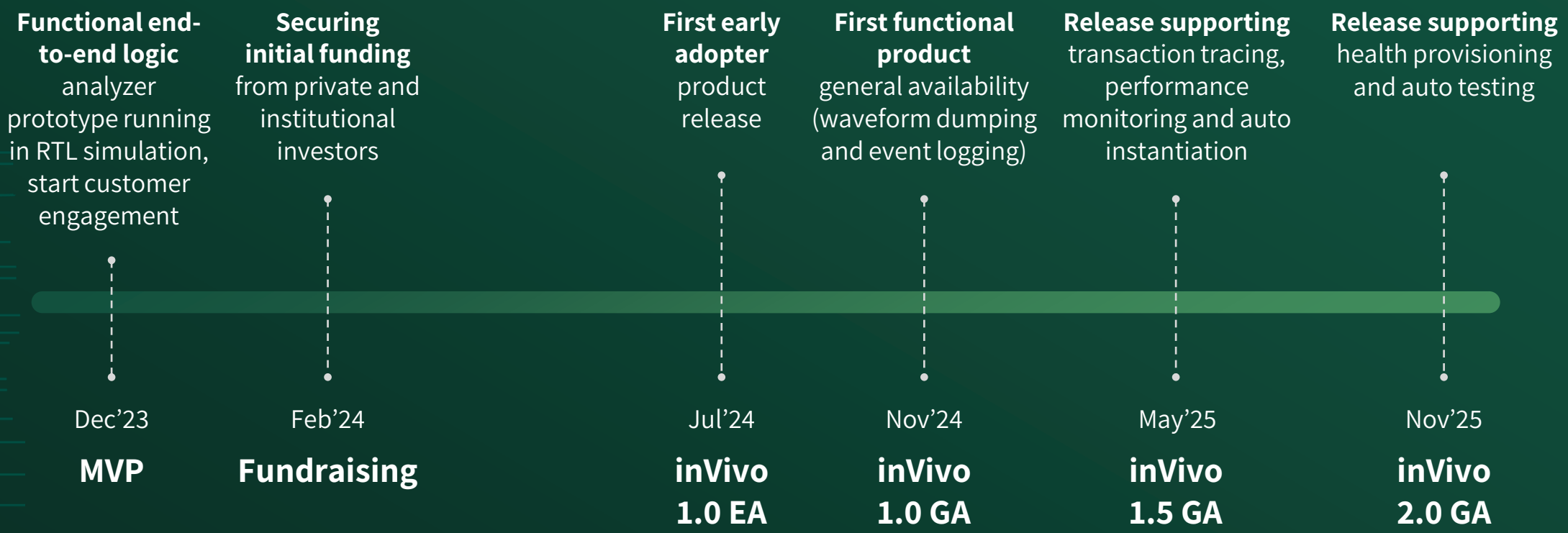
SEQUANS · intel · SAMSUNG · BROADCOM · SCKIPIO · COPPERGATE

MeaTech · CANNOVA · BIOLIGHT · GEFEN BIOMED INVESTMENTS · Micromedic · Anchiano therapeutics · HORIZON GreenTech Ventures · Meytav · ATI

ADC BERLINSIDERS · NITSBA GROUP · AROUNDTOWN SA · TLG IMMOBILIEN

BioCanCell · Anchiano therapeutics · Novobatt · Steakholder FOODS

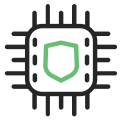
Roadmap


Functional end-to-end logic analyzer prototype running in RTL simulation, start customer engagement
Dec'23
MVP
Securing initial funding from private and institutional investors
Feb'24
Fundraising
First early adopter product release
Jul'24
inVivo 1.0 EA
First functional product general availability (waveform dumping and event logging)
Nov'24
inVivo 1.0 GA
Release supporting transaction tracing, performance monitoring and auto instantiation
May'25
inVivo 1.5 GA
Release supporting health provisioning and auto testing
Nov'25
inVivo 2.0 GA

Improved product time to-market

Streamlining silicon debug

Acceleration
of chip bringup time



Shortening SW development
by enhancing chip visibility

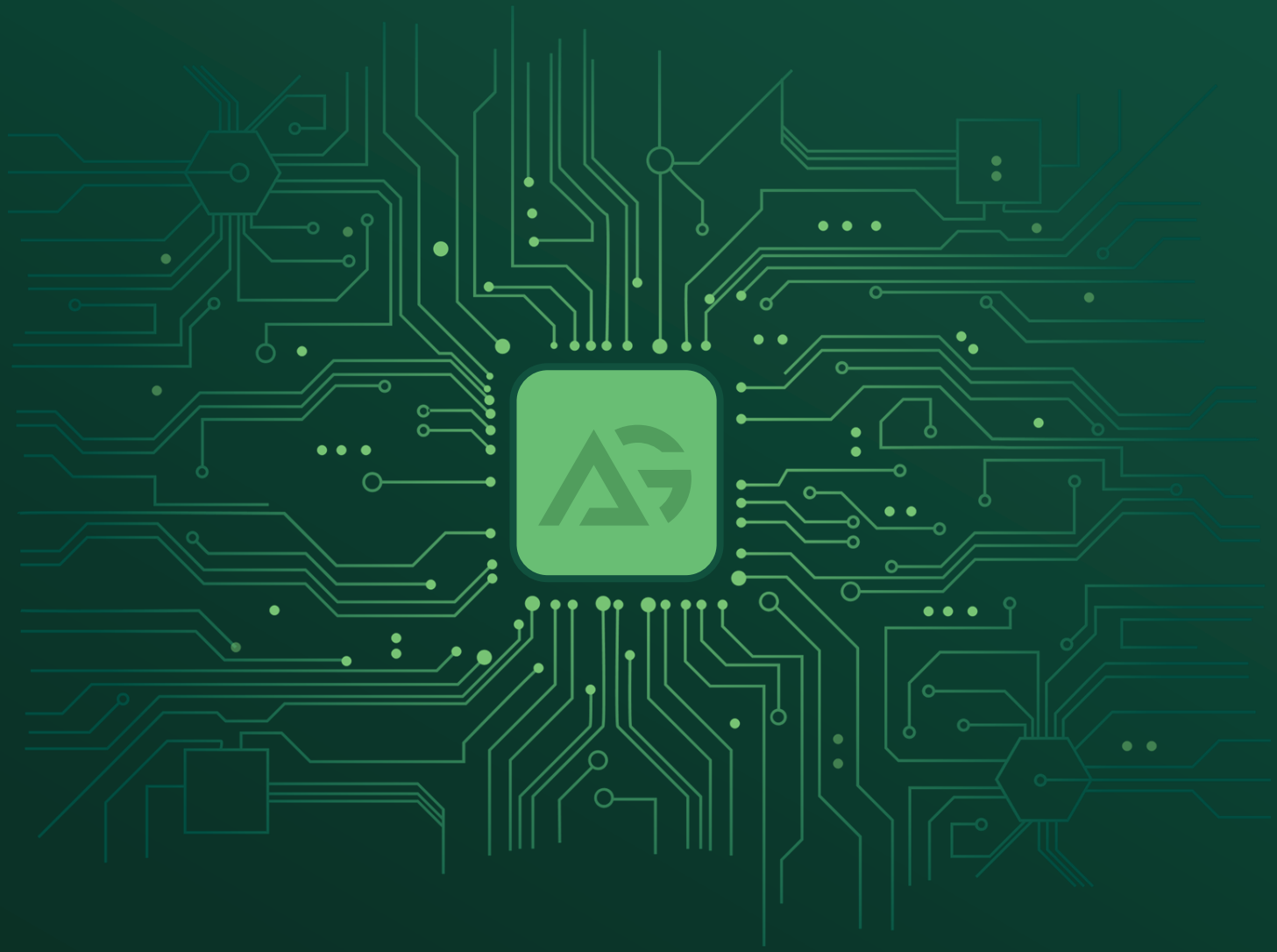
Advanced performance analysis
for system tuning

Adding intelligence into chip debugging

Automatic identification
of irregularities

Back-tracing
source problems

Automatic analysis
of system performance



AsicGram

The Gold Standard for Silicon Debug

Contact Us:

Arik Shmayovitsh

Mobile: +972-52-5421144

email: arik@asicgram.com

Exit Strategy

Mellanox TECHNOLOGIES

Internal use
(est. ~10sM$)
2017

SIEMENS

ultraSOC

Pivot into automotive
(est. ~10sM$)
2020

Public IP Companies

ARTERIS IP

2022
Revenue
$50M

Market Cap
$197M

CEVA

2022
Revenue of
$135M

Market Cap
$406M

Cash Flow Projection